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speed cache memory. When a memory request is generated, the request is first presented to the cache memory, and if the cache cannot respond, the request is then presented to main

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memory. The difference between cache and virtual memory is a matter of implementation; the two notions are conceptually the same because they

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L3 cache is a segment of overall cache memory. L3 cache is faster than RAM but

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slower than L2 cache.

To further fasten up the process cache of second order L2 cache are used. They are located at immediate vicinity of processor.

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spilling (due to register pressure: register to cache), cache miss (cache to main memory), and (hard) page fault (main

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